REMARKS

Reconsideration of this application is respectfully requested in view of the following remarks.

Claims 3 and 7-11 are pending in this application and subject to examination.

In the Final Office Action mailed March 21, 2006, claims 8, 10 and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wang et al. (U.S. Patent No. 6,448,820, hereinafter "Wang") in view of the Applicant's Admitted Prior Art (hereinafter "AAPA"). Claims 3, 7 and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wang in view of Hanke, III et al. (U.S. Patent No. 5,376,848, hereinafter "Hanke") further in view of the AAPA. The Applicant hereby traverses the rejections, as follows.

Claims 8, 10 and 11 Rejected under 35 U.S.C. § 103(a)

Claims 8, 10 and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wang in view of the AAPA. The Applicants respectfully submit that the combination of Wang and the AAPA fails to disclose or suggest each and every feature recited in claims 8, 10 and 11.

In the Amendment filed February 15, 2006, claim 8 was amended to clarify that the divider is configured to divide a frequency of the output signal by a division rate, wherein a frequency of a signal output from the divider is less than a frequency of the input signal so as to determine how frequent a signal phase is adjusted. In addition, claim 10 was amended to clarify that the frequency of the output signal is divided by a division rate, such that the frequency of a signal obtained by the division is less than a

frequency of the input signal so as to determine how frequent a signal phase is adjusted.

Thus, in the Applicant's invention as recited in independent claims 8 and 10, the frequency of a delayed signal is divided by a division rate such that the divided frequency is less than the frequency of the delayed signal. By dividing the frequency of the delayed signal to decrease the frequency, the claimed delay time adjusting circuit determines how frequently a signal phase is adjusted.

As acknowledged by the Examiner, Wang does not teach a dummy circuit to delay an output of the divider by a fixed delay time. The Examiner relies on the AAPA as teaching a dummy circuit, and asserts that it would have been obvious for one of ordinary skill in the art to incorporate the dummy circuit of the AAPA into the delay adjusting circuit of Wang. However, Wang also does not teach or suggest adjusting a delay time of the input signal so as to match the phases of a signal input to an input buffer that supplies the input signal to the delay adjusting circuit (PLL circuit) and a signal output from an output buffer that outputs an output signal from the PLL circuit.

Neither Wang nor the AAPA teaches or suggests dividing a frequency of the output signal by a division rate, wherein a frequency of a signal output from the divider is less than a frequency of the input signal so as to determine how frequently a signal phase is adjusted, as recited in claims 8 and 10. Thus, the combination of Wang and the AAPA fails to disclose or suggest each and every feature recited in independent claims 8 and 10. As such, claims 8 and 10 are neither anticipated nor rendered obvious by the combination of Wang and the AAPA.

Further, the Applicant submits that if the signal output from the output buffer were fed back to the PLL circuit via a dummy circuit, the performance of the PLL circuit would deteriorate when the output pattern is not a constant toggle between high and low levels. Accordingly, it would not have been obvious for those skilled in the art to use a dummy circuit in Wang.

For at least these reasons, the Applicant submits that independent claims 8 and 10 are allowable over the applied art of record.

Claim 11 depends from claim 9 and is allowable for at least the reasons set forth below with respect to claim 9.

Claims 3, 7 and 9 Rejected under 35 U.S.C. § 103(a)

Claims 3, 7 and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wang in view of Hanke, and further in view of the AAPA. The Applicants respectfully submit that the combination of Wang, Hanke and the AAPA fails to disclose or suggest each and every feature recited in claims 3, 7 and 9.

In the Amendment filed February 15, 2006, independent claim 7 was amended to clarify that the first divider is configured to divide a frequency of the input signal by a first division rate so as to determine a target that is used to adjust a signal phase, and that the second divider is configured to divide a frequency of the output signal by a second division rate higher than the first division rate so as to determine how frequent the signal phase is adjusted. In addition, independent claim 9 was amended to clarify that a frequency of an input signal is divided by a first division rate so as to determine a target that is used to adjust a signal phase, by selecting a number of delay units in a delay

chain, the input signal is delayed to output an output signal, and a frequency of the output signal is divided by a second division rate higher than the first division rate so as to determine how frequently the signal phase is adjusted.

As explained above, Wang fails to teach a dummy circuit. Further, as acknowledged by the Examiner, Wang also fails to teach or suggest two dividers having mutually different division rates, i.e., a second divider having a higher division rate than a first divider which receives an input signal. Hanke is cited as allegedly teaching two dividers having mutually different division rates, but fails to teach or suggest a dummy circuit. The Examiner relies on the AAPA as teaching a dummy circuit that is not taught by Wang or Hanke. However, similar to Wang, as explained above, Hanke also fails to teach or suggest adjusting a delay time of the input signal so as to match the phases of a signal input to an input buffer that supplies the input signal to the delay adjusting circuit (PLL 10) and a signal output from an output buffer that outputs an output signal from the PLL circuit.

None of Hanke, Wang and the AAPA, nor any combination thereof, discloses or suggests at least the combination of determining a target that is used to adjust a signal phase by dividing a frequency of an input signal by a first division rate, delaying the input signal to output an output signal, and determining how frequently the signal phase is adjusted by dividing a frequency of the output signal by a second division rate higher than the first division rate, as in the invention recited in independent claims 7 and 9. Thus, the combination of Wang, Hanke and the AAPA fails to disclose or suggest each and every feature recited in independent claims 7 and 9. As such, claims 7 and 9 are

neither anticipated nor rendered obvious by the combination of Wang, Hanke and the AAPA.

Further, if the signal output from the output buffer were fed back to the PLL circuit via a dummy circuit, the performance of the PLL circuit would deteriorate when the output pattern is not a constant toggle between high and low levels. Accordingly, it would not have been obvious for one of ordinary skill in the art to use a dummy circuit in Hanke.

For at least these reasons, the Applicant submits that independent claims 7 and 9 are allowable over the applied art of record.

As claims 7 and 9 are allowable, the Applicant submits that claims 3 and 11, which depend from claims 7 and 9, respectively, are likewise allowable for at least the reasons set forth above with respect to claims 7 and 9.

Conclusion

For all of the above reasons, it is respectfully submitted that claims 3 and 7-11 are in condition for allowance and a Notice of Allowability is earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is invited to contact the undersigned representative at the telephone number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300 referencing client matter number 100353-00037.

Respectfully submitted,

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Enclosure: Petition for Extension of Time (one month)